Top-Down Fabrication of Fully CMOS-Compatible Silicon Nanowire Arrays and Their Integration into CMOS Inverters on Plastic

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ABSTRACT A route to the top-down fabrication of highly ordered and aligned silicon nanowire (SiNW) arrays with degenerately doped source/drain regions from a bulk Si wafer is presented. In this approach, freestanding n- and p-SiNWs with an inverted triangular cross section are obtained using conventional photolithography, crystal orientation dependent wet etching, size reduction oxidation, and ion implantation doping. Based on these n- and p-SiNWs transferred onto a plastic substrate, simple SiNW-based complementary metal-oxide-semiconductor (CMOS) inverters are constructed for the possible applications of these SiNW arrays in integrated circuits on plastic. The static voltage transfer characteristic of the SiNW-based CMOS inverter exhibits a voltage gain of ~9 V/V and a transition of 0.32 V at an operating voltage of 1.5 V with a full output voltage swing between 0 V and V_{DD}, and its mechnical bendability indicates good fatigue properties for potential applications of flexible electronics. This novel top-down approach is fully compatible with the current state-of-the-art Si-based CMOS technologies and, therefore, offers greater flexibility in device design for both high-performance and low-power functionality.

KEYWORDS: silicon nanowire · CMOS compatibility · ion implantation · field-effect transistor · CMOS inverter · plastic

Plastic electronics is one of today's most significant emerging technologies that promises to form the basis of the next generation of electronic and photonic systems.[1] The potential applications for plastic electronics include flat-panel displays, electronic papers, smart cards, and wearable displays.[2−7] The active materials for devices on plastic, amorphous silicon, organic semiconductors, and polycrystalline silicon have been intensively explored; however, the low carrier mobilities exhibited by amorphous silicon and organic semiconductors and the high-temperature annealing process required for achieving high-quality polycrystalline silicon restrict their potential use in applications where high performance and low power are required.[2,4,6−12] Furthermore, lack of controlled doping techniques presents a challenge for integrating these materials into various device architectures. Recently, substantial efforts have been made to construct semiconductor devices on plastic by utilizing inorganic semiconductor nanomaterials as the active components.[13−17] Because of the unique physical, electrical, and optical properties, semiconductor nanowires (NWs) are drawing increasing attention as the active building blocks for assembling a variety of nanoscale devices at the end of the roadmap and beyond.[18−22] Among the various semiconductor NWs, silicon NWs (SiNWs) are particularly attractive, due to the well-established knowledge of silicon and silicon-related materials, such as silicon dioxide and silicon nitride, and even more importantly, due to their compatibility with the current Si-based ultra-large-scale integration (ULSI) technology.[23,24] In general, SiNWs can be achieved using one of two distinct approaches: "bottom-up" and "top-down". Compared with the bottom-up-synthesized SiNWs, the top-down approach, in which bulk materials are reduced in size to nanoscale patterns using advanced lithography tools, enables the controlled assembly of the SiNWs into well-ordered arrays at precise locations for the implementation of integrated electronic and photonic systems. Several research groups made use of this top-down approach to obtain SiNWs *via* different nanopatterning techniques, including electron beam lithography (EBL) combined with electrochemical size reduction,[25] atomic force microscopy (AFM) nanolithography based on local oxidation,[26] and nanoimprint lithography (NIL).[27] However, most of these techniques have the following drawbacks: (1) incompatibility with the current Si-based complementary metal-oxide-semiconductor (CMOS) technologies, (2) low throughput capability unsuitable for high-volume mass production, and (3) economic issues caused by the high cost of silicon-on-insulator (SOI) wafers.

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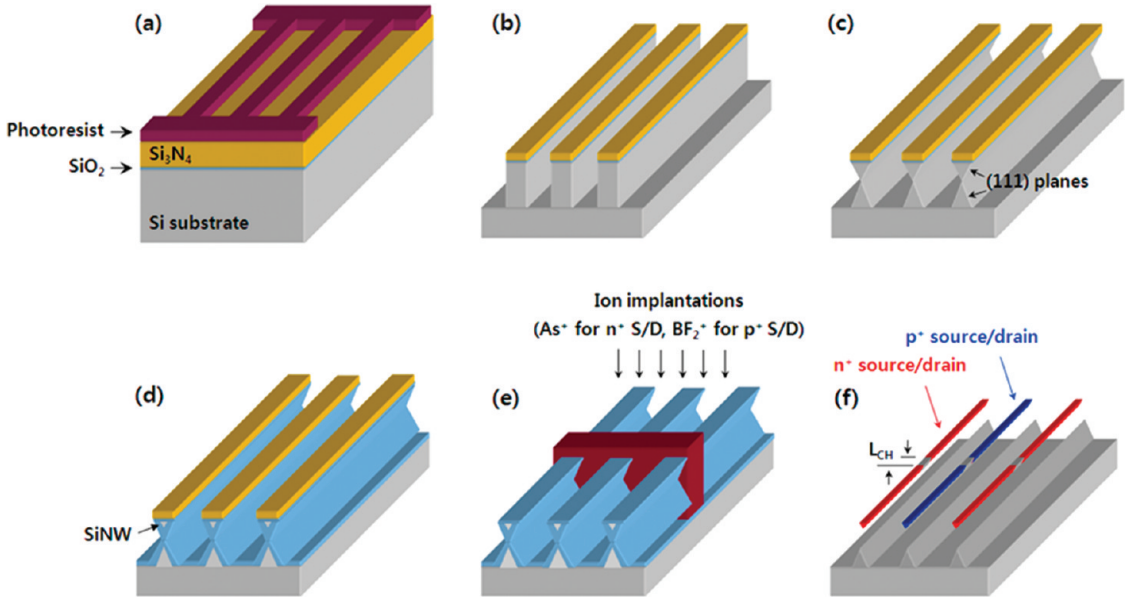

Figure 1. Key process steps used to obtain the freestanding complementary SiNW arrays with degenerately doped source/drain regions from a bulk Si wafer. (a) Definition of Si active regions along the [110] direction after pad oxidation with a thickness of 10 nm and nitride deposition with a thickness of 150 nm. (b) Si trench etching using the nitride film as a hard mask. (c) Crystallographic wet etching in 25 wt % TMAH solution to obtain the inverted triangle-shaped Si lines. (d) Thermal oxidation of the Si lines for reducing the dimension of the SiNWs down to sub-100 nm. (e) Source/drain implantations with As^+ and BF_2^+ ions for n- and p-SiNWs, respectively, followed by activation annealing. (f) Release of the SiNWs *via* wet chemical etching using BOE solution.

Herein, we develop a route to the top-down fabrication of highly ordered and aligned SiNW arrays with degenerately doped source/drain regions from a bulk Si wafer by using fully CMOS-compatible Si technologies, which include conventional photolithography, crystal orientation dependent wet etching, size reduction oxidation, and ion implantation doping. This novel top-down approach is fully compatible with the current Si-based CMOS technologies and, therefore, offers greater flexibility in device design for both high-performance and low-power functionality.

RESULTS AND DISCUSSION

There is a need to assemble electrically uniform and reproducible SiNW arrays into CMOS devices on plastic using the existing semiconductor fabrication facilities that have device performance comparable to the conventional MOS field-effect transistors (MOSFETs) on single-crystalline substrates. Our approach has several key features that make it promising for SiNW-based CMOS applications on plastic. First, using the well-established CMOS technologies for macro- and nanopatterning, high-quality single-crystalline SiNW arrays can be achieved from bulk Si wafers, enabling superior control over the location, density, and alignment of the SiNW arrays. Since these SiNW arrays are suspended over a Si substrate, they can be readily transferred onto plastic substrates. Second, unlike most SiNW devices, in which metal contacts are commonly used, the use of degenerately doped source/drain contacts eliminates the need for high-temperature annealing steps to improve the contact properties. Indeed, these annealing steps are incompatible with the process temperatures required for the use of plastic, because most plastics deform or melt at temperatures of 100−200 °C. In addition, because all of the high-temperature SiNW fabrication steps, such as thermal oxidation, low-pressure chemical vapor deposition (LPCVD), and dopant activation annealing, are conducted before the device fabrication stages, there is no need to be concerned with the thermal limitations caused by the use of plastic. Finally, as the size of MOSFETs is scaled down to the nanoscale regime, they suffer from issues associated with static power consumption, due to the increase in the off-state subthreshold leakage.[28,29] To address these issues, novel device concepts based on alternative working principles, such as tunneling FETs (TFETs)[30] and impact-ionization MOS (I-MOS) transistors,[31] have been proposed to achieve a sub-60-mV/dec subthreshold swing. In this regard, our approach provides greater flexibility in device design by means of precise control over the type and concentration of the dopant through ion implantation. For example, by using ion implantation to accurately introduce the dopants with specific types and concentrations for the source and drain regions of the SiNWs in turn with separate photomasks, SiNW MOSFETs can be integrated with SiNW TFETs and/or I-MOS transistors on one chip to achieve both high-performance and low-power functionality.

Figure 1 illustrates the fabrication procedure used to obtain the freestanding complementary SiNW arrays

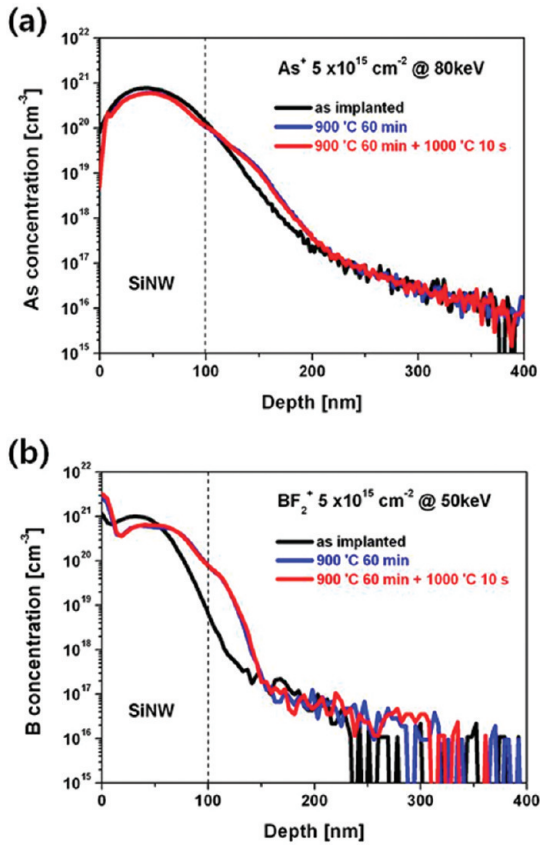

Figure 2. SIMS analysis. (a) Arsenic profiles with 5×10^{15} cm^{-2} dose of As^+ ions for the source/drain of the n-SiNWs. (b) Boron profiles with 5×10^{15} cm^{-2} dose of BF_2^+ ions for the source/drain of the p-SiNWs. The profiles were analyzed before and after the thermal steps: as-implanted, after activation annealing at 900 °C for 60 min, and RTA at 1000 °C for 10 s. The analysis was performed with a double-focusing magnetic sector mass spectrometer (CAMECA IMS-7f) using a 10 kV Cs^+ primary beam for arsenic and a 10 kV O_2^+ primary beam for boron.

with degenerately doped source/drain regions from a bulk Si wafer. The starting wafer was a p-type (100)-oriented Si bulk wafer with a resistivity of 8−12 Ω·cm. First, a 10 nm thick pad oxide was grown on the Si surface, and a 150 nm thick nitride film was then deposited by LPCVD. The pad oxide layer serves not only as a stress relief layer to diminish the stress-induced dislocations that a nitride film exerts in the Si surface, but also as a screen oxide layer to minimize the channeling during ion implantation. The role of the thin nitride film is threefold: a hard mask layer for etching the Si substrate, a hard mask layer for protecting the SiNWs from the wet chemical solution, and an oxygen diffusion barrier during thermal oxidation for reducing the dimensions of the SiNWs. Next, the Si active regions were defined along the [110] direction by photolithography (Nikon, NSR-2005i10C) (Figure 1a). After the plasma etching of the pad oxide and the nitride film followed by the stripping of the photoresist, the Si substrate was etched anisotropically until the desired trench depth was reached (Figure 1b). By using the nitride film as a hard mask, crystallographic wet etching in 25 wt % tetramethylammonium hydroxide (TMAH) solution was performed to obtain the inverted triangle-shaped Si lines (Figure 1c). The TMAH is favored over potassium hydroxide (KOH) because of its compatibility with the CMOS process, as it does not contain harmful alkali ions. Because the etch rate of the (111) plane is much slower than that of the (100) and (110) planes, it can act as an etch stop. As a result, the inverted triangle-shaped Si lines aligned along the [110] direction are produced. This crystal orientation dependent wet etch process is based on the fact that while both the (100) and (110) planes have two dangling bonds per unit cell, the (111) plane has only one dangling bond per unit cell.[32] The Si structure with two connected Si lines forms an hourglass-like structure in which the upper part of the Si lines can be used as a SiNW after the size reduction oxidation process. Following the formation of the inverted triangle-shaped Si lines, thermal oxidation of the Si lines was carried out in a wet ambient to reduce the size of the SiNWs down to the sub-100 nm range (Figure 1d). Then, the wafer was dipped into 50:1 buffered HF (BHF) solution to remove the thin oxide layer grown on the nitride film during the previous size reduction oxidation step. After that, the nitride film was completely stripped in hot phosphoric acid at a temperature of 160 °C. During the stripping of the nitride film, the surrounding oxide can also be etched by hot phosphoric acid, but the high etch selectivity of the nitride film to the surrounding oxide in hot phosphoric acid makes it possible to protect the SiNWs safely. In order to make the source and drain regions of the SiNWs doped, As^+ ions with a dose of 5×10^{15} cm^{-2} and BF_2^+ ions with a dose of 5×10^{15} cm^{-2} were implanted as n- and p-type dopants at ion energies of 80 and 50 keV, respectively, after the source and drain regions for n- and p-SiNWs were defined in turn with separate photomasks (Figure 1e). Optionally, using additional photolithography and ion implantation steps, lightly doped drain (LDD) regions of the SiNWs can be formed to improve the short channel reliability. Compared with the diffusion doping process used previously,[33,34] the ion implantation doping process has the benefits of being able to precisely control the dopant concentration and projected range for the optimization of the doping profiles. Then, the wafer was first annealed at 900 °C for 60 min in nitrogen ambient in order to ensure a uniform dopant diffusion in the body of the SiNWs and then annealed at 1000 °C for 10 s in a rapid thermal annealing (RTA) system. In the final step, forming gas annealing was performed at 450 °C for 30 min. As a result of removing the surrounding oxide *via* wet chemical etching using buffered oxide etchant (BOE) solution, the SiNWs were released from the Si substrate and, thus, highly ordered and aligned freestanding complementary SiNW arrays with a controlled pitch and density were formed (Figure 1f).

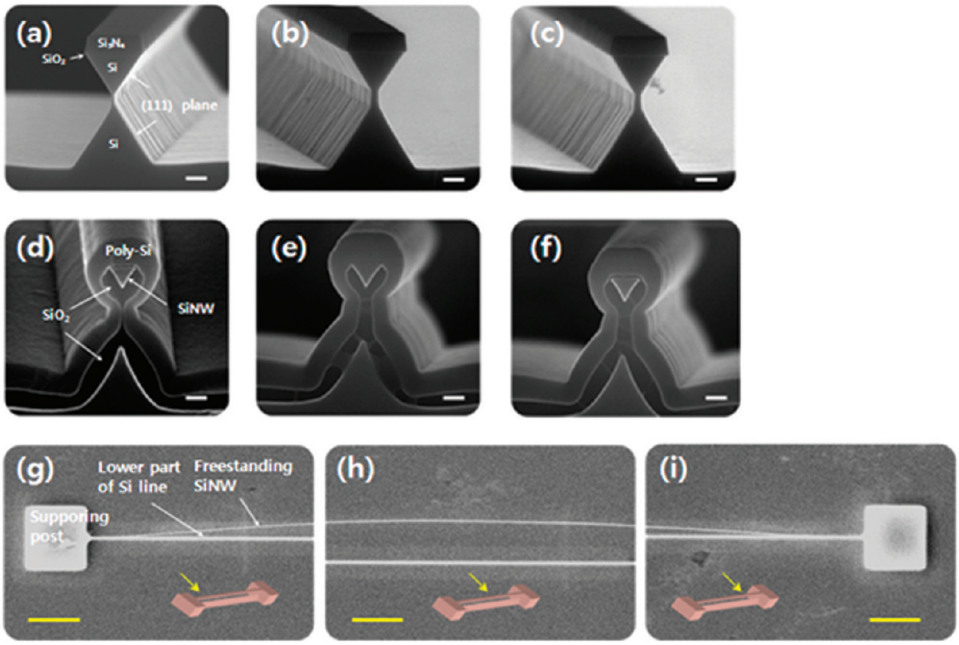

Figure 3. SEM images taken after the key process steps shown in Figure 1. (a−c) Cross sections of the inverted-triangle-shaped Si lines obtained by TMAH wet etching. The scale bars are 100 nm. (d−f) Cross sections of the SiNWs obtained by using size reduction oxidation. The scale bars are 100 nm. The three SEM images in a−c and d−f were taken at the top, center, and bottom locations of the Si wafer, respectively. (g−i) Plane-view images of the freestanding SiNW obtained by removing the surrounding oxide, which were taken at the halfway point between two supporting posts and at the two end points near these posts. The scale bars are 5 μm.

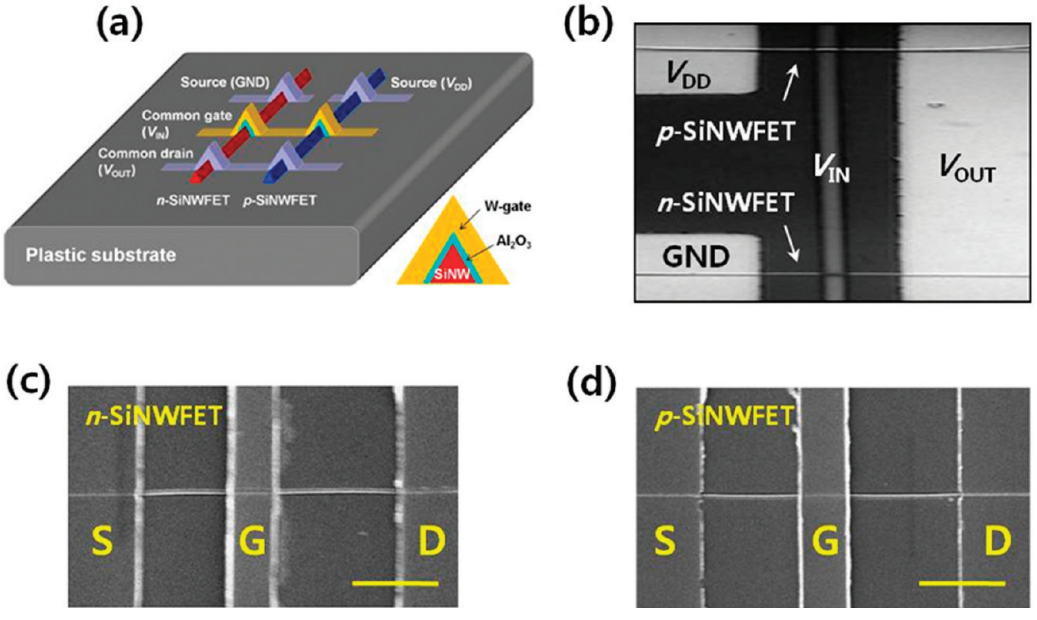

Figure 4. CMOS inverter based on the n- and p-SiNWFETs on plastic. (a) Schematic- and (b) plane-view optical microscope images of the SiNW-based CMOS inverter. The source of the p-SiNWFET is connected to V_{DD}, the power supply voltage, and that of the n-SiNWFET is connected to GND, the ground potential. The drains of both the n- and p-SiNWFETs are connected together to the output node. The input voltage is connected to the gate terminals of both the n- and p-SiNWFETs. (c, d) Plane-view SEM images of the top-gate n- and p-SiNWFETs constituting the CMOS inverter, respectively. The scale bars are 5 μm.

Figure 2 shows the results of secondary ion mass spectroscopy (SIMS) analysis for arsenic and boron profiles before and after thermal steps, *viz.*, as-implanted, after activation annealing at 900 °C for 60 min, and RTA at 1000 °C for 10 s. It is confirmed that the arsenic and boron concentrations at the source/drain regions for the n- and p-SiNWs after the thermal steps, respectively, are above 10^{20} cm^{-3} along the entire SiNW bodies.

The scanning electron microscopy (SEM) images taken after the key process steps are shown in Figure 3. Figure 3a–c shows the cross sections of the inverted-triangle-shaped Si lines obtained by TMAH wet etching, which corresponds to the process step depicted in Figure 1c. Three SEM images per wafer were taken at the top, center, and bottom locations, respectively. The upper part of the Si lines, which is used as the SiNW, has a width and height of about 280–300 and 180–200 nm, respectively. The width of a Si neck at the top location, which connects the upper and lower parts of the Si lines, is measured to be about 20 nm, which is narrower than those at the center and bottom locations (~40 nm), probably due to the nonuniformity of the lithography critical dimension (CD) and/or due to the variation of the TMAH wet etch rate across the wafer. The cross sections of the SiNWs obtained by the size reduction oxidation process are shown in Figure 3d–f. In order to distinguish the clear SiNW from the surrounding oxide layer, chemical staining using BOE solution after the deposition of 150 nm thick poly silicon was performed. The SEM images reveal that the SiNWs are completely surrounded by the oxide layers and that they have an inverted triangular cross section with a height and width of about 100 nm. Note that the Si necks are thoroughly oxidized, so that the SiNWs are electrically isolated from the Si substrate. Using stress-limited oxidation at a low temperature, the diameter of the SiNWs can be further reduced down to the sub 10 nm range, because the buildup of stress during the oxidation prevents the SiNWs from oxidizing away completely.[35] In order to release the SiNWs from the Si substrate, the surrounding oxides were thoroughly removed using BOE solution. Figure 3g–i shows the plane-view SEM images of the freestanding SiNW taken at the halfway point between two supporting posts and at the two end points near these posts. In the middle part, the SiNW is completely separated from the lower Si substrate lines (Figure 3h), while the SiNW at the two end parts clings to the supporting posts (Figure 3g,i). Therefore, the freestanding SiNWs are electrically isolated from the Si substrate and easily transferred onto a plastic substrate.

CMOS logic gates have unique advantages over pure n- or p-type logic gates. One of the most important advantages is that the static power consumption of the CMOS logic gates is negligible, because one of the n- and p-type transistors is always turned off when the gate is in either of the two logic states. The other advantage of the CMOS logic gates is that a full signal swing between GND and V_{DD} with a sharp transition can be achieved. Kim *et al.* demonstrated CMOS logic gates and ring oscillators on plastic using n- and p-type single-crystalline ribbons of Si.[34] With n- and p-type SOI wafers as the starting materials, the doped Si ribbons were fabricated using phosphorus and boron

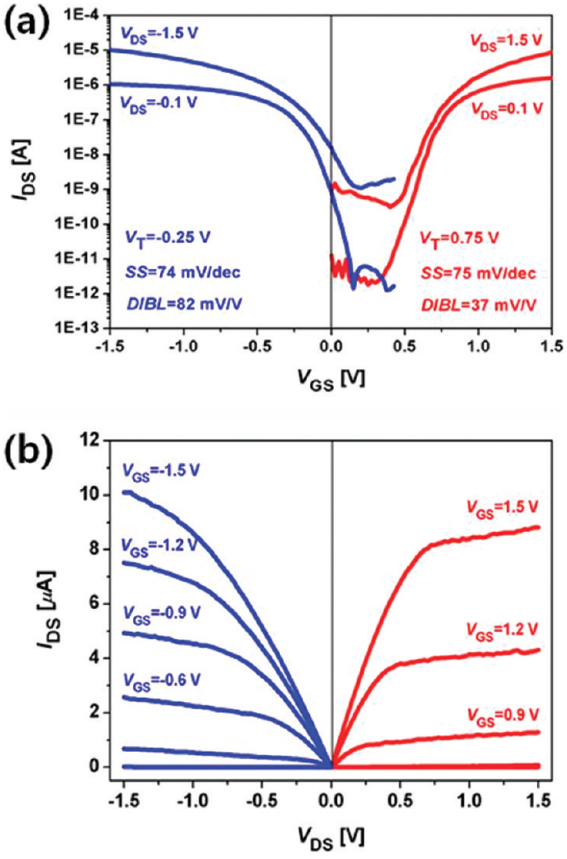

Figure 5. Electrical characteristics of the individual n- and p-SiNWFETs constituting the CMOS inverter. (a) I_{DS} *versus* V_{GS} transfer plots and (b) I_{DS} *versus* V_{DS} output plots of the n- and p-SiNWFETs.

spin-on dopants as the n- and p-type doping for the source and drain. Yet, to date, few studies of CMOS logic gates on plastic using doped SiNWs with full CMOS compatibility have been reported. To the best of our knowledge, this is the first time that CMOS inverters have been constructed on plastic by using fully CMOS-compatible single-crystalline SiNWs with degenerately doped source and drain regions from bulk Si wafers.

A schematic of the SiNW-based CMOS inverter on plastic and its plane-view optical microscope image are shown in Figure 4a,b. The source of the p-SiNWFET is connected to V_{DD}, the power supply voltage, and that of the n-SiNWFET is connected to GND, the ground potential. The drains of both the n- and p-SiNWFETs are connected together to the output node. The input voltage is connected to the gate terminals of both the n- and p-SiNWFETs, and thus, both SiNWFETs are driven directly by the input signal. Figure 4c,d shows the plane-view SEM images of the top-gate n- and p-SiNWFETs constituting the CMOS inverter, respectively. The channel length (L_{CH}) of the p-SiNWFET is designed to be 1.0 μm, which is shorter than that of the n-SiNWFET (L_{CH} = 2.0 μm) to compensate for the low value of the hole mobility. Since the n- and

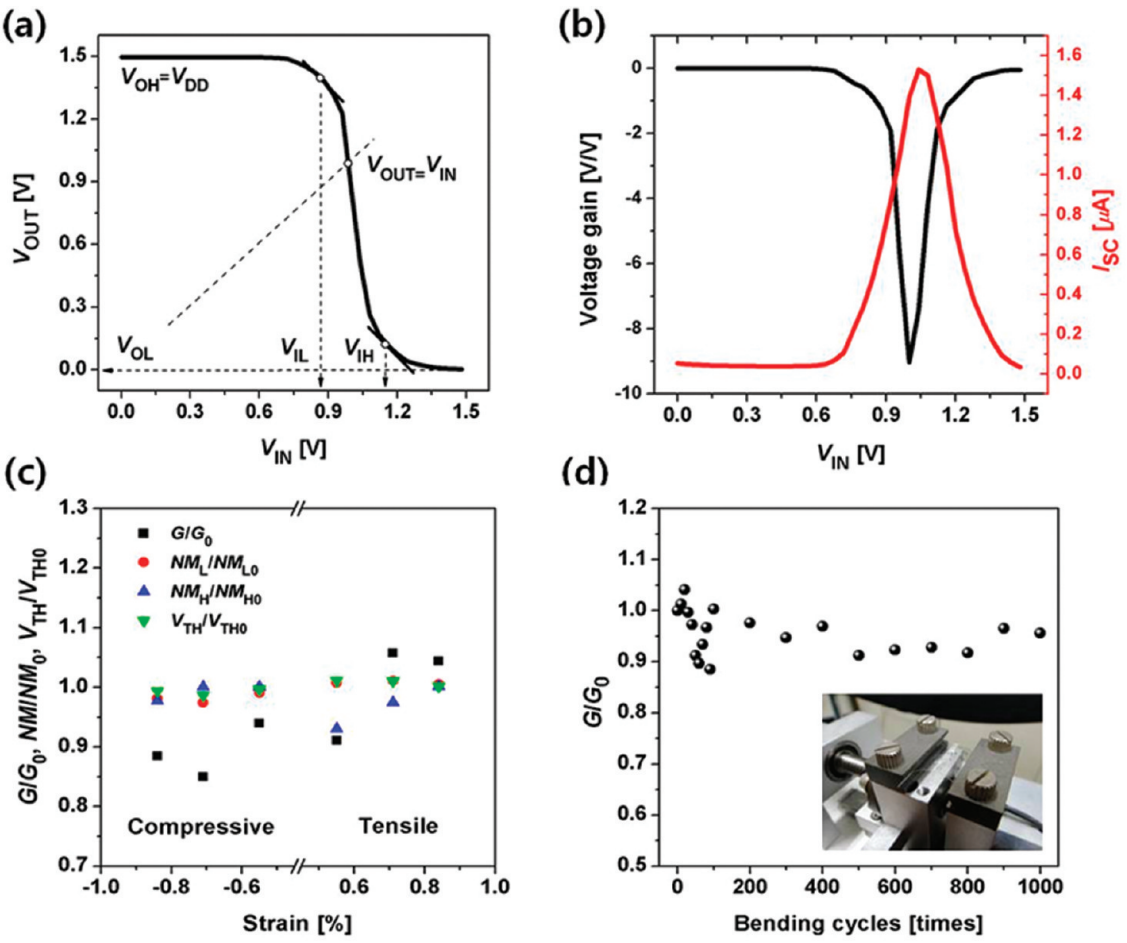

Figure 6. Static characteristics of the SiNW-based CMOS inverter and its mechanical properties. (a) VTC plot and (b) characteristic plots of the voltage gain and power supply current for V_{DD} = 1.5 V. (c) Normalized voltage gain (G/G_0), noise margin (NM_L/NM_{L0} and NM_H/NM_{H0}), and inverter threshold voltage (V_{TH}/V_{TH0}) as a function of bending-induced strains. (d) Normalized voltage gain as a function of bending cycles (of up to 1000 times). The fatigue test was carried out under the applied tensile strain of 0.84%. The inset is the photograph of the sample on a bending (tensile strain) stage.

p-SiNWs were fabricated using the same p-type Si wafer, the n-SiNWFET is operated in inversion mode, while the p-SiNWFET is operated in accumulation mode.

We first characterized the electrical properties of the individual n- and p-SiNWFETs constituting the CMOS inverter. Shown in Figure 5 is the $I_{DS}-V_{GS}$ and $I_{DS}-V_{DS}$ plots for the n- and p-SiNWFETs. On-state currents of 8.8 and 10.1 μA are obtained from the n- and p-SiNWFETs at an operating voltage of 1.5 V, respectively, with an off-state current of a few nA. The threshold voltages (V_T) measured at a drain current of I_{DS} = 100 nA are 0.75 and −0.25 V for the n- and p-SiNWFETs, respectively. Since the difference in V_T between the n- and p-SiNWFETs affects the symmetry in the pull-up and pull-down characteristics of the CMOS logic gates, it is necessary to adjust the V_T values of both the n- and p-SiNWFETs. This can be done by either V_T-adjustment implantation or gate work function engineering. With the twin-well approach, two separate SiNWs for the n- and p-SiNWs can be formed in a lightly doped substrate. Since the doping profiles of each of the SiNWs can be optimized independently, the performance of the n- and p-SiNWFETs is expected to be symmetrical. As an alternative approach, a combination of two metal gates with different work functions can also be used for the n- and p-SiNWFETs, respectively. The drain-induced barrier lowering (DIBL) is 37 mV/V for the n-SiNWFET and 82 mV/V for the p-SiNWFET. The subthreshold swing (SS), defined as the change in the gate voltage required to reduce the subthreshold current by one decade, is extracted to be 75 mV/dec for the n-SiNWFET and 74 mV/dec for the p-SiNWFET using the simple expression $SS = [d(\log 10|I_{SD}|)/dV_{GS}]^{-1}$. The SS values obtained for these SiNWFETs are close to the theoretical limit of 60 mV/dec ($2.3 \times k_BT/q$) at room temperature, indicating that the gate exerts strong control over the channel region and the Al_2O_3 gate dielectric exhibits high thermal stability with the SiNWs. These low values of SS enable the operation of the SiNWFETs with a much lower value of V_T while maintaining the required off-state leakage specification. In turn, a low V_T enables supply voltage scaling while maintaining the performance.

The electrical and mechanical characteristics of the CMOS inverter based on these n- and p-SiNWFETs are shown in Figure 6. From the static voltage transfer characteristic (VTC) for V_{DD} = 1.5 V shown in Figure 6a, five critical voltages are extracted: the input low voltage (V_{IL} = 0.86 V), input high voltage (V_{IH} = 1.18 V), output low voltage (V_{OL} = GND = 0 V), output high voltage (V_{OH} = V_{DD} = 1.5 V), and inverter threshold voltage ($V_{TH} \equiv V_{IN}$ at ($V_{OUT} = V_{IN}$) = 0.98 V). The VTC has a noise margin for low signal levels ($NM_L = V_{IL} - V_{OL}$) and noise margin for high signal levels ($NM_H = V_{OH} - V_{IH}$) of 0.86 and 0.32 V, respectively. The VTC exhibits a full output voltage swing between 0 V and V_{DD} and a sharp transition of 0.32 V. Figure 6b shows the voltage gain characteristics of the SiNW-based CMOS inverter and the power supply current as a function of the input voltage. The voltage gain of the VTC, defined as the maximum slope of the transition between the high and low voltage states, is about 9 V/V for V_{DD} =1.5 V, and the current being drawn from the power supply voltage during the transition reaches a peak value of about 1.5 μA when $V_{IN} = V_{TH}$; that is, the maximum current is drawn when both the n- and p-SiNWFETs are operating in saturation mode. In the study carried out by Wang *et al.*, the SiNW-based CMOS inverter was fabricated using the superlattice nanowire pattern transfer (SNAP) process combined with the pattern doping technique.[33] Compared favorably with the results of Wang *et al.*, which had a low voltage gain of ~5 V/V and a wide transition width of ~1 V for V_{DD} = 3 V, our results show the better switching performance with full signal restoration for the lower operating voltage of 1.5 V. To investigate mechanical properties of the CMOS inverter consisting of the n- and p-SiNWFETs, we performed systematic tests by bending the plastic mechanically along the channel transport direction to achieve the convex (or tensile) and concave (or compressive) surface strain values between 0.55% and 0.84% [see Supporting Information, Figure S1]. The applied strain values were estimated by using the bending curvature radius and plastic substrate thickness. For this range of strains, only small changes in CMOS inverter characteristic parameters, such as voltage gain, noise margin, and inverter threshold voltage, are observed, as shown in Figure 6c. In addition, Figure 6d shows that the voltage gain changes by less than 15% after bending cycles up to 1000 times under the applied tensile strain of 0.84%, indicating that the SiNW-based CMOS inverter has good fatigue properties.

Further experiments are being conducted to verify that our approach for fabricating complementary SiNW arrays is useful for plastic electronics applications by improving the performance of the n- and p-SiNWFETs. In addition, memory devices and more complex logic circuits, such as NAND, NOR gates, and ring oscillators, are being fabricated to realize integrated circuits on plastic substrates on a much larger scale as a step toward commercial applications.

CONCLUSION

In summary, we developed a reliable and controllable route to the top-down fabrication of highly ordered and aligned n- and p-SiNW arrays with degenerately doped source/drain regions from a bulk Si wafer by using fully CMOS-compatible Si technologies, including conventional photolithography, crystal orientation dependent wet etching, size reduction oxidation, and ion implantation doping. This novel top-down approach offers several key features that make it promising for plastic electronics applications: (1) superior control over the location, density, and alignment of the SiNW arrays, (2) no concern about the thermal budget limited by the use of plastic, and (3) flexibility in device design for high-performance and low-power functionality. Using these as-aligned n- and p-SiNWs transferred onto plastic, we constructed a SiNW-based CMOS inverter on plastic, which has good electrical and mechanical properties for potential applications of low-power flexible electronics. Although the performance does not reach the level of the current state-of-the-art CMOS inverter on single-crystalline substrate, this study is meaningful in that it is the first report on the integration of fully CMOS-compatible SiNW arrays into the CMOS inverter on plastic.

EXPERIMENTAL SECTION

CMOS Inverters on Plastic. The construction of a SiNW-based CMOS inverter on plastic begins with the transfer of the as-aligned n- and p-SiNWs onto a plastic substrate [see Supporting Information, Figure S2]. A 50 nm thick ultraviolet (UV)-curable resin (Q-sys, NIR Q1) with the low viscosity of 6.5 cps at 25 °C, which is a liquid photopolymer that cures when exposed to UV light, was laminated on the plastic by a spin-coating process (Figure S2a). Then, the plastic coated with the UV-curable resin was brought into conformal contact with a donor Si chip containing the n- and p-SiNWs under controlled temperature and contact pressure (Figure S2b). Since the viscosity of the resin used for transfer of the SiNWs is low, the SiNWs are anchored on the surface of the plastic, not on the surface of the resin, by surface adhesion between two substrates. Subsequently, after the resin was hardened by UV light exposure, the crystalline connections to the supporting post at the ends of the SiNWs were broken when the donor Si chip was detached from the plastic, bringing the n- and p-SiNWs with the plastic (Figure S2c). Finally, the resin layer was completely removed by immersing it in ethanol solution, leaving the n- and p-SiNWs on the plastic by the van der Waals interactions with the surface of the plastic (Figure S2d). To bring the representative n- and p-SiNWs on the plastic into contact with

the metal source/drain electrodes, the patterned source/drain regions of the n- and p-SiNWs were deposited using Al (60 nm) and Au (40 nm) metals after BHF treatment and subsequently rinsing in deionized water to remove native oxides and promote the formation of ohmic contacts. Then, a 10 nm thick Al_2O_3 gate dielectric layer was deposited on these SiNWs using atomic layer deposition. In the final step, the definition of the gate regions over the n- and p-SiNW channel regions was followed by the deposition of 100 nm thick W metals to form the gate electrode.

SIMS Analysis. The analysis was performed with a double-focusing magnetic sector mass spectrometer (CAMECA IMS-7f) using a 10 kV Cs^+ primary beam for arsenic and a 10 kV O_2^+ primary beam for boron.

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Supporting Information Available: Mechanical properties of the SiNW-based CMOS inverter on bending and method for transferring the SiNWs from a donor Si chip to the plastic. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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